ABSTRACT

Long Term Evolution (LTE) is a technology that has been released by 3GPP with the ability to achieve data transmission speeds of 100 Mbit / s for downlink and 50 Mbit / s for uplink. LTE technology is designed to provide better spectrum efficiency, increased radio capacity, latency and low operating costs for operators as well as mobile wireless broadband services of high quality to users. LTE is intended as a comprehensive network solutions and secure communication with data rates much higher. For the needs of data rate and high throughput on LTE, the most suitable coding technique is turbo coding. The advantages of Turbo Code is the minimum power usage at each modulation that allows the transmission of signals with very low power levels.

Based on the above explanation, it is in this final project to design a prototype Turbo Code decoder circuit that used in LTE technology using software Xilinx ISE Design Suite 14.5 with the coding language VHSIC Hardware Description Language (VHDL) and then be implemented on a Field Programmable Gate Array (FPGA) board ATLYS Spartan-6 XC6SLX45 CSG324C.

From the results indicated that the design of a prototype implementation of Turbo Decoder can be done on board ATLYS Spartan-6 XC6SLX45 CSG324C. The results indicate the implementation of resource usage by 23% on the FPGA board. This results in a system prototype with a minimum period of 19.662 ns and frequency of work under the working frequency of the Spartan-6 FPGA, namely 50.963 MHz.

Key Words: **LTE**, ***3GPP, Turbo Code, FPGA***