ABSTRACT

New series of FPGA has more memory, register, and logic component than the old one. Pipeline computation which was not popular because need a lot of resource of FPGA, is now possible to realize. Telecommunication research based on VHDL-FPGA has to move from serial computation to pipeline computation because now we have a big number of resources in single FPGA chip.

This research designs an OFDM-STBC modulator with 16-QAM Mapping on transmitter side. The OFDM system uses IFFT-1024 5 stages with radix-4 formula in it and the STBC system is designed for 4x4 antennas with code rate ½ which each 4 symbols will be transmitted, each antenna send 8 symbols in a period of time. Pipeline computation method is used in designing the whole system which two focuses of this method are time synchronization applied by control generator block and data freezer at the end of each block. All blocks in this research are applied using VHDL language and implemented in Kintex-7 XC7K325T-3FFG900 FPGA. Mapping, STBC, and IFFT work process are simulated by Ms.Excel and verified by Matlab. VHDL code is created using Altium Designer and simulated in Modelsim with Ms.Excel as verifier. VHDL code then loaded into FPGA using Xilinx ISE 14.2 and analyzes using Chipscope.

Simulation result of integration all blocks verified by Matlab does not show any error. But implementation result shows that there is error occured in IFFT and or STBC block. Realization OFDM-STBC and 16-QAM mapping using 17 bits of fixed point data type, require 65% slice registers, 17% slice LUTs, 557 of 303959 of fully used LUT-FF pairs, 21% bonded IOBs, 1% Block RAM, 40% BUFG/BUFGCTRLs, and 8% DSP48E1s of FPGA resource. Using 100 MHz of internal clock FPGA will result 50 Mbps system bit rate.

Keyword : FPGA, Pipeline, 16-QAM, IFFT-1024, STBC 4x4, VHDL.