

## ***Abstract***

*Currently, NUMA cache coherence protocols already implemented, one of which MOESI CMP Token. However, another problem arises in the form of a cache miss rate is greater with increasing number of processors. Therefore, in this thesis, measured as the number of processor performance using a simulator gem5 increasingly combined with TOPAZ and two kinds of benchmarks. The other parameters are measured in the form of execution time, throughput, latency, and average memory access time.*

*Results obtained from these simulations is the addition of processor capable of reducing the execution time of the whole process while encouraging maximum throughput benchmarks apply to both. The local memory will be more than the maximum time accessing memory on another node. Percentage acceptance or data packets reach 39-40% in the 4-CPU and 31-32% on an 8-CPU. As an exception to the addition of 16-CPU found the maximum percentage of 26% packet reception.*

*Keywords: NUMA, gem5, TOPAZ, latency, cache coherence, cache miss rate*