Abstract

The development of modern electronic equipment currently has a sophisticated functionality but also has a small size. This was triggered by the entry into force of Moore's Law so that the processing capacity of a chip can be increased. However, this processing capacity needs to be balanced by design productivity. One way to overcome the complexity of system design is to raise the level of abstraction of a system.

Traditional design flow modeling Register Transfer Level (RTL) is not able to meet the time to market. In this case a higher level of abstraction necessary for designers to explore the design space at the system level. Transaction Level Modeling (TLM) is an approach with a level of abstraction higher than RTL.

RTL and TLM has a different style of modeling, therefore the result of both this model are compared to determine the functionality of the model built. In this thesis, a model is single-purpose processor to calculate the least common multiple. From RTL and TLM modeling results, both have shown that the functionality goes well.

Keywords: *embedded system, Register Transfer Level, Transaction Level Modeling, SystemC.*