PERANCANGAN DAN IMPLEMENTASI LINEAR PRECODING LTE ARAH DOWNLINK BERBASIS FPGA

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Abstrak

Precoding adalah bentuk umum dari beamforming untuk mendukung transmisi multi layer pada sistem multi antena untuk komunikasi wireless. Beamforming adalah sebuah teknik pemrosesan sinyal yang digunakan pada sensor arrays untuk sinyal direksional baik pada sisi transmitter atau penerima. Pada single-layer beamforming, sinyal yang sama ditransmisikan dari setiap antena dengan pembobotan yang proporsional sehingga sinyal dapat termaksimasi pada output penerima. Ketika penerima merupakan multi antena, single-layer beamformingtidak dapat secara simultan memaksimalkan level sinyal pada antena penerima. Sehingga, untuk memaksimalkan throughput pada sistem multi antena, dibutuhkan multi-layer beamforming.

Tugas Akhir ini akan merancang sebuah sistem precoding linier LTE pada sisi transmitter. Sistem precoding tersebut akan dibuat dalam kode VHDL dan akan diimplementasikan pada FPGA. Pada Tugas Akhir ini, precoding terdiri dari 64-QAM Mapper sebagai input, blok precoding, dan dihubungkan dengan OFDM (IFFT) block. Precoding direncang dengan skenarion mode transmisi (Transmission Mode - TM) 6 pada LTE release 9 dan akan menggunakan codebook standar 3GPP sebagai matriks precoding untuk TM 6 pada MIMO 2x2.

Hasil dari Tugas Akhir ini menunjukkan bahwa precoding mengurangi kompleksitas sistem deteksi pada sisi penerima. Proses implementasi menunjukkan bahwa hasil Tugas Akhir ini dapat di implementasikan pada hardware dan akan menggunakan 62% occupied slice, 11% slice register, 48% 4 input LUTs, 27% Bounded IOBs, and 9% BUFG/BUFGCTRLs resource FPGA dengan total 2021 clock, 121 clock untuk proses delay dan 1900 clock untuk sekali proses simbol OFDM, dan memiliki bitrate 161,68 Mbps.

Kata Kunci : Linear precoding, codebook FPGA, VHDL, MIMO

Abstract

Precoding is a generalization of beamforming to support multi-layer transmission in multi-antenna wireless communications. Beamforming is a signal processing technique used in sensor arrays for directional signal transmission or reception. In conventional single-layer beamforming, the same signal is emitted from each of the transmit antennas with appropriate weighting such that the signal power is maximized at the receiver output. When the receiver has multiple antennas, single-layer beamforming cannot simultaneously maximize the signal level at all of the receive antennas. Thus, in order to maximize the throughput in multiple receive antenna systems, multi-layer beamforming is required.

This Final Project is building a LTE linear precoding system for the transmitter side. The precoding system will be built in VHDL code and will be implemented on FPGA. In this Final Project, the precoding sistem consists of 64- QAM Mapper as input system, and will be connected to OFDM (IFFT) block. The precoding is built based on Transmission Mode (TM) 6 of LTE release 9 and will be using 3GPP codebook standard as the precoding matrix for TM 6 for 2x2 MIMO.

The Final Project shows that by the used of linear precoding system in transmission, it decreases the complexion of detection system in precoding block on the receiver side. The implementation process shows that the Final project is implementable on hardware and will use 62% ocupied slies, 11% slice register, and 27% of bounded IOBs resources of FPGA. with 2021 clock in total process, 121 clock in delay process and 1900 clocks to produce one OFDM symbol. The bitrate of the system is 161,68 Mbps.

Keywords : Linear precoding, codebook, FPGA, VHDL, MIMO

CHAPTER 1
INTRODUCTION

1.1 Motivation

Multimedia communications has developed rapidly for last decades. As multimedia communications become increasingly popular, mobile communications are expected to reliably support high data rate transmissions. In this way, many improvements have been made during these past years through several generations of mobile communication systems.

Recently, the 3rd Generation Partnership Project (3GPP) has reached a mature state in the specification of Long Term Evolution (LTE) standardization. This new standard, also known as the fourth generation of mobile network systems, allows the use of a couple of new technologies which give the opportunity to have high capabilities compared to previous generations. Since the end of 2009, LTE mobile communication systems started to be deployed as the next generation of mobile communication. It is considered as a natural evolution of previous generations known as Global System for Mobile communications (GSM) and Universal Mobile Telecommunications System (UMTS).

One of the common feature of LTE is the using of MIMO (Multiple Input Multiple Output) antennas. MIMO is the use of multiple antennas at both the transmitter and receiver to improve communication performance. MIMO can be sub-divided into three main categories, precoding, spatial multiplexing or SM, and diversity coding. Precoding is a generalization of beamforming to support multi-layer transmission in multi-antenna wireless communications. In conventional single-layer beamforming, the same signal is emitted from each of the transmit antennas with appropriate weighting such that the signal power is maximized at the receiver output. When the receiver has multiple antennas, single-layer beamforming cannot simultaneously maximize the signal level at all of the receive antennas. Thus, in order to maximize the throughput in multiple receive antenna systems, multi-layer beamforming is required.

The previous work has built LTE encoder system for 2x2 MIMO antennas, but it has no precoder system yet. This Final Project is expected to complete the precoding system of LTE by using linear precoding method which is completed

by the use of codebook matrix. The precoder will be built in VHDL language and will be implemented on FPGA board.

1.2 Problem Formulation

The problem formulation for this Final Project are:

1. Designing LTE precoder with VHDL
2. LTE precoder implementation on FPGA
3. Testing and checking the result of designed LTE precoder implementation on FPGA.

1.3 Objectives

The objective of this Final Project is to design a LTE precoding system in VHDL and implement it on FPGA which includes:

1. Simulation of linear precoding LTE.
2. The implementation of linear precoding in digital circuit and determining the resources utilization included CLB, Slice, and DSP48.
3. The analysis of data rate in linear precoder system.

1.4 Scope of Work

1. Baseband level system.
2. This ungraduated thesis is focused on LTE Precoder designing.
3. The design will only be including transmitter part of LTE
4. The Final Project is using the 6th Transmission Mode of LTE which is specified for slow moving user (0-10 km/hour velocity).
5. Perfect syncronization is assumed.
6. Using FPGA hardware for Xilinx Virtex XC4VLX25-SF363.
7. The validation of designed system will be using Isim of Xilinx software and Microfsoft Excel 2007.

1.5 Methodology

This Final Project is arranged by following method:

1. Literature studies by collecting information about precoder LTE from relevan journals, books, articles, and other references.
2. System planning including the making of system design, building the system design, and doing the implementation of the design result.
3. Bulding the architecture design on VHDL using Xilinx software and verify the output using Matlab software.
4. Implementing the designed system on FPGA.

1.6 Outline of the Report

Chapter 1 Introduction

Introduction chapter will include the background, problem formulation, objectives, scope of work, and methodology of this Final Project.

Chapter 2 Literature of Review

This chapter describes the basic concept of the topics for this Final Project taken from books, academic journals, and other reliable resources.

Chapter 3 Design and Implementation of System

This chapter describes the architecture of the system in detail, including the modeling, the block diagrams, and the flowcharts of the designed system.

Chapter 4 Analysis and Implementation of Precoding System

This chapter describes the implementation process the designed system, the result of the implementation, and the analysis of the system implementation.

Chapter 5 Conclusion and Recommendation

This is the final chapter of this Final Project. The chapter describes the final conclution of the Final Project and the recommendation for future project.

CHAPTER 5
CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

This Final Project can be concluded as listed below.

1. The design system has meet the requirement of the desired system. It generates 161,68 Mbps bitrate on simulation and implementation stage with 100 MHz clock frequency.
2. Precoding block system implementation requires 1% occupied slice, 1% slice register, 1% 4 input LUTs, 27% Bounded IOBs, and 6% BUFG/BUFGCTRLs of FPGA resources.
3. Precoding block system that has been connected to the OFDM block requires 62% occupied slice, 11% slice register, 48% 4 input LUTs, 27% Bounded IOBs, and 9% BUFG/BUFGCTRLs of FPGA resources.
4. The system is succesfully implemented on FPGA Virtex-4 XC4VLX25-SF363 board with above requirement by the help of chipscope software from Xilinx. The implementation shows the same result with the simulation on Isim software.

5.2 Recommendation

Further research can be done by developing some points listed as below.

1. Building precoding on the receiver side and the tranmission channel for precoding detection and real pmi feedback value.
2. Building complete precoding structure including layer mapper and resource element block.
3. Using codebook for MIMO 4x4.
4. Using different mapper constallation. For example 16-QAM or 256 QAM.

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