ABSTRACT

Modern digital communication systems are now reliable in dealing with noise and interference on the transmission channel. Channel coding method is one important solution to support that capability. Convolutional code is one of the channel coding method, which has been used in WiMAX technology (802.16e) and DVB (Digital Video Broadcasting). This is because the reliability of the transmission channel suitable convolutional code with high noise and sending data bit stream.

At the end of the task has been designed and implemented system convolutional encoder decoder code with code rate 1/3 constraint lenght 3, sequence generator 5 (101), 7 (111), and 7 (111), and trace back the number of input bits is 8 bits (1 Byte) on the decoder side. This means that the decoder is capable of correcting one bit error maximum of 2 bits of mutual sequence of data sent in a stream. Encoder and Decoder Program consists of four input ports and one output port, to issue the serial output bits. Then performed on the design language VHDL and then the design is implemented on FPGA Virtex 4 XC4VLX25.

After implementation on FPGA, including the block encoder and decoder obtained the amount of resource required is the amount of 4% slice, slice the number of flip - flops 1%, the 5 input LUT 1%, the number of bonded IOB 2%, and the gate used is 920 gates

Key Words : *Channel Coding, Viterbi code rate 1/3*, FPGA