ABSTRACT

Telecommunication system aims to transmit the signal from the source to the desired destination. At first, the development of information sources were only in form of voice and Short Message Service (SMS) with a low bandwidth. As it developed, information sources can be in form of images, video and data services with much wider bandwidth. Modulator is needed to process the signal from information sources so that it can be transmitted through the canals. 64 QAM modulator is one type of modulator that has higher bit rate than ASK, FSK, or PSK modulator.

In this research, 64-Quadrature Amplitude Modulation (QAM) is designed by using Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL). Bits of sources information is paralleded into bits *inphase* and *quadrature*. Then the bits is represented in form of symbol constellation with various amplitude and phase. Modulator modulates the constellated information signal with the carrier signal which is in the form of sine and cosines signal. The simulation is done in ModelSim SE 6.3f software and is implemented on the Development Board Vitrex 4 XC4VLX25 SF363 Field-Programmable Gate Array (FPGA) by Xilinx ISE Design Suite 12.1 software.

The modulator output is represented in the form of 64 symbols with various *inphase* and *quadrature*. The system implementation is using 1% resource of Virtex 4 XC4VLX-SF363. This shows that the system can be implemented properly without any overload. This modulator takes 2400 clock delay. The frequency of the internal clock of Virtex 4 XC4VLX-SF363 is 10 ns, so this modulator has 41,667 kHz frequency and 250 Kbps bit rate.

Key Word : 64-QAM, Digital Modulation, FPGA, VHDL.