ABSTRACT

Heart attack is number one cause of human dead in the world. In purpose of controlling the number of death caused by heart attack monitoring the condition of heart is very important. ECG is an interpretation of the electrical activity of the heart over time captured and externally recorded that can detect the condition of heart and trouble on it. An ECG signal has QRS complex as it main component. So, detecting the value of QRS complex is very important in the way get the information of heart conditions. Pan-Tompkins method is the most wide common use in hardware implementation of QRS complex detector.

This research's goal is to implement the hardware that can be use in detecting the value of QRS complex. The future implemented hardware will be supplied by ECG signal that has been converted to digital signal before by an Analog to Digital Converter (ADC). Operation to ADC output signal will be handled by programmed FPGA that run the operating as the Pan-Tompkins method. This research implement in FPGA due to its flexibility in programmed and also the price is relative cheaper than other hardwares that commonly use nowadays.

In Pan-Tompkins method the implemented system will be consist by several block, they are band pass filter block, derivation block, squaring operation block, integration block and decision block. The blocks will be implemented on FPGA as calculating operation blocks system that consists of adder, resister, address loader, memory and also control unit.

As the result, this project successfully produces QRS detection system with 92% accuracy ang 245 ms processing time delay within clock of 5 ms.

Keywords: Electrocardiograph, Pan-Tompkins, complex QRS, ADC, FPGA