

## ABSTRACT

To achieve good service, especially in the reception of signals, then one very important thing to be done by operators is to extend antenna's beam to the users without expand it to the direction of other users who can be as an iterferer. If this can be done, so the increasing of transmit power efficiency of the antenna will be obtained. In addition, efforts should also be done to reduce the impact of interference derived from other operators or network capacity and impact derived from the wave propagation characteristics.

Earlier, one technique that can be used to solve the above problem is to use smart antenna systems or adaptive antennas. The radiation patterns of smart antenna always vary according to the current condition of the radio and the user's position. Main lobe of the radiation pattern will only be directed to user, while the side lobe and null lobe will be directed to the interference signals. Thus, the power consumption will be more efficient. In addition, the radiating power from the base station will be further so the coverage area will increase.

This paper explain the implementation of RLS (Recursive Least Square) algorithm for signal processing in smart antenna using a Programmable Logic Device FPGA device Virtex4 XC4VLX25. From the results obtained by implementations have been done, the information about the amount of FPGA resources used in this research reach 654% which means need up to 7 FPGA Virtex4 XC4VLX25 to realize this design. This because the system uses large number of multiplier and adder circuit to do calculation of large dimension matrix.

The weight values produced by RLS algorithm in this research are able to produce maximum Array Factor value for array antenna with error of 1,19526% so generally, it can be said that RLS algorithm can be used for CDMA.

**Keywords :** radiation pattern, smart antenna, RLS, CDMA, VHDL, FPGA