ABSTRACT

In modern communication system, the need of synchronize information between sent data and received data are very high. Noise and interference in transmission channel that has been sent sometimes become a problem that made received information contains some errors. Channel coding is one of so many processes that can be held to solve the problem because the use of channel coding is to guard the information from noise and interference. Implementation of channel coding could be error detection or error correction.

Reed-Solomon code is one of the good techniques for channel coding. By using this code, error from the information can be detected and corrected. Reed-Solomon codes that used in this final project is Reed-Solomon (15,9). This code using 15 symbols of codeword and 6 symbols of parity that means this code could correct up to 3 error symbols.

After the implementation in FPGA has been done, we can get some conclusions such as in encoder block, resources needed of slices is 1%, amount of *slice flip – flops needed is* 1%, amount of 4 input LUT needed is 1%, amount of *Bonded* IOB needed is 1%, and total gates used is 2950 *gates*. In decoder block, resources needed of slices is 20%, amount of *slice flip – flops needed is* 4%, amount of 4 input LUT needed is 18%, amount of *Bonded* IOB needed is 2%, and total gates used is 29584 *gates*

Keywords : *Channel Coding*, *Reed-Solomon*, FPGA.