ABSTRACT

Along with modern technology, digital wireless communication system is demanded to serve high data rate with reliable QOS (small BER with minimum SNR). Various noise on wireless communication is a problems. It makes mistakes of receive data in receiver side increased.

LDPC is a encoding technique which is proper with Forward Error Correction system. Fourier transform on LDPC is used to decrease complicated on decoding process. LDPC code is defined as sparse parity check matrix code and hoped by sending high-bit-rate will produce the low bit error probability. Sparse parity check matrix is parity check which has low closing bit. It is called low density parity check because it behavior that has more 0 (zero) than 1 (one) on parity check matrix.

The main predominance of this technique is LDPC can producing performance which has closing value to various channel (Shannon Limit) and it have linear decoding process.

LDPC use code rate ½ to produce great performance for communication system. By using iteration system on decoder, LDPC produce low error bit value on various SNR condition.

Requirement on designing this project is using VHDL (VHSIC (*Very High Speed Integrated Circuit*) *hardware description language*) language and to synthesize or to load the logic circuit is by using FPGA (*Field Programmable Gate Array*).