ABSTRACT

In digital communication, transmit the information process from transmitter to receiver, is very sensitive with noise, noise that happen will make error to the data transmitted. For that need a protection from the data that will transmite to error that might happen.

Error that happen from noise, will make the data damage. The damage from the data can be detection and correction through the channel coding process that have a function to give the redundancy bit to data, so if find some error from the information bit, then the receiver can detected and corrected without forward error correction. In this paper will make the implementation of differential cyclic code 11 bit, the subclass of cyclic code is using feedback shift register. Difference-set cyclic code encoder(transmitter) will make codeword u(x) from data that transmited using polynomial generator g(x). Detection and correction process will be perform by using syndrome s(x). While the codeword that receive by receiver r(x), is a codeword that transmited u(x) add by error pattern e(x) that happen.

From the result of simulation and implementation, Cyclic code can detect and correction of maximum 2 bits in 21 bits of codeword. And for the clock of decoder, it must be 5 faster from the clock of encoder. This design will made by VHDL (VHSIC(Very High Speed Integration Circuit) Hardware Description Language) and will be simulated by Aldec Active-HDL 3.5, then synthesis by Xilinx ISE 8.1, and the target device is the FPGA(Field Programmable Gate Array)

Keywords : *Difference-set cyclic code, FPGA.*