ABSTRACT

In a digital communications system there are transmitter, channel of transmission and receiver like at communications system generally. And at a receiver generally there are functioning demodulator to dissociate the information signal from the carrier signal. There is a part of demodulator that called the signal detector. A good signal detector is a detector that capable to follow the fluctuation of clock rate and also has low noise.

The others performances of a digital communications is also determined by several things, one of them is synchronization. There are synchronization of symbol timing, synchronization of carrier and also clock synchronization .

A particular circuit that called Symbol Timing Recovery (STR) is needed to do the synchronization of symbol timing. This STR circuit is used to trigger the integrator and dump circuit block and also sampling and hold circuit block inside of the signal detector, so that the sampling rate will be equal to the input signal bit rate.

In this final project have been done the designing of NRZ-bipolar detector using STR circuit block to improve the quality of output signal. As well as have been determined the types and also the values of proper component to get the optimal performances of NRZ-bipolar detector, by using software “Multisim 9” as a means of assist for the simulation of.

The simulations result shows that delay that happened between the input signal and the output signal of NRZ – bipolar detector is about 11,178 µs (0,71 Tb). And at the output signal of NRZ-bipolar detector circuit happened the enlargement pulse for the bit of '1' becoming 15,865 µs (1,015 Tb) from which ought to be 15,625 µs. While for the bit of '0', the pulse width is 15,625 µs, so that is not happened the enlargement and also the stricture of pulse width.