ABSTRACT

Shannon Entropy computation is a fundamental concept in information theory that is important for various applications, yet its hardware implementation presents unique challenges, particularly in logarithmic operations and the handling of fractional numbers. This research aims to design, implement, and verify a digital hardware architecture for Shannon Entropy computation optimized for the FPGA platform. This architecture is implemented using the Verilog Hardware Description Language (HDL) with a modular approach controlled by a Finite State Machine (FSM). For resource efficiency, the design utilizes fixed-point representation to handle arithmetic operations on fractional numbers and leverages a ROM-based Look-Up Table (LUT) method to quickly approximate the logarithm function. The functional verification process is conducted in the ModelSim simulation environment using an EEG dataset. The simulation results from the hardware design are then validated by quantitatively comparing them against a golden reference value generated by MATLAB with high precision. The verification results show a very high correspondence between the entropy value calculated by the design and the reference value from MATLAB, where a very small error margin was identified as a natural quantization error resulting from precision conversion, thus proving that the proposed architecture is valid and functions accurately.

***Keywords**: Shannon Entropy, FPGA, Digital Design, Verilog, Fixed-Point, Look-Up Table, Functional Verification.*