ABSTRACT

This research discusses the x86 architecture and the use of *cache* memory in computer systems. *Cache* memory plays an important role in improving the efficiency and performance of computer systems by storing frequently used data. There are three types of *cache* in the processor, namely L1 *Cache*, L2 *Cache*, and L3 *Cache*, each of which has a different size and function. The commonly used *cache* replacement policy is Least Recently Used (LRU), but this policy is inefficient in managing the *cache* in situations where there are fluctuations between critical saturation and unsaturation states. Therefore, the Tree Pseudo Least Recently Used (TreePLRU) method is proposed as a more efficient solution in managing the *cache* with changing access patterns. This research uses the gem5 simulator to perform modeling and simulation of computer architecture performance. Tests were conducted using matrix multiplication as the standard of comparison. The test is measured by the success and failure rate of the *cache* (*cache* hit and *cache miss*). The result of this research is expected to know the comparison of *cache* hit and *cache miss* on *cache* replacement policy using TreePLRU and LRU on x86 architecture.

Keywords: *Least Recently Used (LRU), Tree Pseudo Least Recently Used (TreePLRU),* gem5*, cache hit, cache miss.*