ABSTRACT

Along with the development of technology and information, sending data from one part to another part is very easy to do. In digital data transmission from the transmitter to the receiver, a process of data security and noise cancelling process has a very important role. Steganography is a technique for data security by hiding data into other data in a different format, the original format was only known by those who know the key . Except, format data security processes, noise cancelling which will be sent also has a same interests. Noise cancelling aims to recover the original data without noise influence will cause the received different data in receivers which transmitted by the transmitter. Removal of noise (noise canceling) is using the Spectral subtraction (SS-Method) which uses a frequency domain method for the removal of noise (noise canceling).

In this thesis, designed a system that aims to eliminate the noise which is stored in the steganography images data into audio. The results of the design are modeled with VHDL programming language (Very High Speed Integrated Circuit Description Language) and simulated by using I-Sim then synthesized and implemented using Xilinx ISE 13.2 Target device used is Virtex 4 XC4VLX25 FPGA-10SF363 with display output through Chipscope Pro Analyzer and GUI (Graphic User Interface) in matlab R20012a.

From the results of modeling and simulation is carried out on a hardware level FPGA synthesis with Xilinx Shynthesize Tools. The synthesis of block noise cancellation obtained the required number of resources is a slice of 2, Slice flip lop 23, LUT 75, IOB 18, FIFO16/RAMB 16 were 38 and GCLK 2. Results at the level of the signal generated by Matlab software resulting MSE values of 0.000999, 0.001284, 0.007383 with PSNR 78.13359, 77.04559, 69.44858.

Keyword: steganography, noice canceller, spectral substraction method, FPGA.