ABSTRACT

FFT (Fast Fourier Transform) is a method of solving discrete signals that are widely used today. For along time FFT is only viewed as a computing system, but now the FFT has become something very important, especially in communication using the BWA (Broadband Wireless Access). So if the FFT works well so does the technology.

In this final project, has designed a processor FFT / IFFT 512 point radix 8 by using the Cooley-Tukey algorithm on an FPGA board, Xilinx Virtex-4 XCVLX25, which aims to prove that the processor FFT / IFFT can be designed on an FPGA which has the same performance with the modeling in MATLAB that it can be used to design applications such as OFDM and other applications. The final project is using VHDL (Very High Speed Integrated Circuit Hardware Description Language) as languages that encode each FFT processor blocks / IFFT 512 point.

Design with this VHDL is modeling system in accordance to the requirements of the system processor FFT / IFFT 512 points and simulate it with ModelSim before the synthesis software translate the design in hardware. Then the simulation results compared with the modeling that has been done in MATLAB. From the results of modeling and simulation,then the synthesis performed at a level hardware with the Xilinx FPGA Tools Shynthesize. From the synthesis results obtained the number of slice and the other parameters including the number of IOB, LUT, Flip-Flop, GCLK, FIFO / RAM and DSP. Overall, this study was able to prove that the processor I / 512 point FFT using radix 8 can be implemented on the FPGA by using minimum resources that give possibility to be developed for the application's development. For testing which needed ADC (Analog to Digital Converter) / DAC (Digital to Analog Converter) block.

Keywords: DFT, FFT, VHDL, FPGA