ABSTRACT

The Highspeed analog-to-digital conveters (ADC) family has become the most popular ADC architecture for sampling rates from a few megasample per second (Msps) up to hundreds Msps. It resolution and sampling reates cover a wide range of applications including CCD imaging, ultrasonic medical imaging , digital receiver, radar (for example GPR) , modems and also assisting the acquisition system.

In this final project, The Highspeed ADC family will be throughly discussed from its early development to the most recent one. Also the mechanism and operation some of them will be expalined for sure. Nowadays, Highspeed ADC of various forms have imporved greatly in speed, resolution, dynamic performance and low power in recent years. One of its kind is pipelined ADC architecture.

Simulator for comperhensive study and analysis of pipelined ADC has been developed and compiled in Wolfram Mathematica 9 for this final project purpose. Users can simulate the input and output process, learning basic principle for some pipelined ADC arcitectures and understanding what are the advantages of ceratain architecture has. The simulator accepts user specified paramters such as ADC's resolution, input voltage values and output data format types. The simulator also works as actual data converter from the PC audio input. It also reads the saved data files from ADS61xx and *.wav* audio format that previously stored.

Keywords: *Analog to digital Converter, Highspeed ADC, Pipeline Architecture, Wolfram Mathematica, ,*