ABSTRACT

In the application of FFT algorithm, computing speed, simple in implementation and memory savers are things that must be considered. For those needs of the most suitable technique for implementation is the pipeline architecture. The advantages of the pipeline architecture is processing data can be parallelized, works in real time, continuous processing and have a little latency.

In this research, the design of FFT by using one of the variants of the technique because the MDC pipeline architecture that is more simple control, the amount of data processed is 64 subcarriers using a radix 2 decimation in frequency for FFT algorithm approach. The design is based on the determined standards. Furthermore, the design is simulated in the ModelSim software. From the results of modeling and simulation then implemented into the FPGA device. The results showed that the design of prototype implementation of FFT algorithm using MDC techniques can be implemented on Spartan-6 ATLYS board.

The implementation results show resource usage slice registers by 3.6%, use of bonded IOBs 10.55%, and a delay process to produce 22900 ns, whereas in previous research in resource usage slice registers at 4.4%, the use of bonded IOBs of 34.4 % and produce 35400 ns delay process. MDC is a solution so that the FFT algorithm implementation in memory efficiency and computing speed. Prototype This results in a system with a minimum period 15.895ns and 62.914 MHz operating frequency.

Keyword : FFT, *Multipath Delay Commutator*, FPGA